IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Method of Forming A Crystalline Phase Material

* * * * *

INVENTORS

Gurtej S. Sandhu
Sujit Sharan

ATTORNEY'S DOCKET NO. MI22-510

TECHNICAL FIELD

This invention relates generally to formation of crystalline phase materials in semiconductor wafer processing and more particularly to formation of refractory metal silicides and crystalline phase transformation thereof.

BACKGROUND OF THE INVENTION

Silicides, such as titanium silicide and tungsten silicide, are commonly utilized electrically conductive materials in semiconductor wafer integrated circuitry fabrication. Such materials are utilized, for example, as capping layers over underlying conductively doped polysilicon material to form electrically conductive lines or interconnects. Such silicide materials are also utilized at contact bases intermediate an underlying silicon substrate and overlying conductive polysilicon contact plugging material. Silicides can be provided by chemical vapor deposition, or by deposition of elemental titanium or tungsten over an underlying silicon surface. Subsequent high temperature annealing causes a chemical reaction of the tungsten or titanium with the underlying silicon to form the silicide compound.

Titanium silicide ($TiSi_2$) occurs in two different crystalline structures or phases referred to as the C49 and C54 phase. The C49 structure is base-centered orthorhombic, while the C54 is face-centered orthorhombic. The C54 phase occurs in the binary-phase diagram while

the C49 phase does not. The C49 phase is therefor considered to be metastable. The C54 phase is a densely packed structure having 7% less volume than the C49 phase. The C54 phase also has lower resistivity (higher conductivity) than the C49 phase.

The C49 phase forms at lower temperatures during a typical refractory metal silicide formation anneal (i.e. at from 500℃ - 600℃) and transforms to the C54 phase at higher elevated temperatures (i.e., greater than or equal to about 650° C). The formation of the higher resistive C49 phase has been observed to be almost inevitable due to the lower activation energies associated with it (2.1 - 2.4 eV) which arises from the lower surface energy of the C49 phase compared to that of the more thermodynamically stable C54 phase. Hence, the desired C54 phase can be obtained by transforming the C49 phase at elevated temperatures.

Due at least in part to its greater conductivity, the C54 phase is much more desirable as contact or conductive line cladding material. Continued semiconductive wafer fabrication has achieved denser and smaller circuitry making silicide layers thinner and narrower in each subsequent processing generation. As the silicide layers become thinner and narrower, the ratio of surface area to volume of material to be transformed from the C49 to the C54 phase increases. This requires ever increasing activation energies to cause the desired transformation, which translates to higher anneal temperatures to effect the desired phase transformation. In some instances, the temperature must be at

least equal to or greater than 800° C. Unfortunately, heating a silicide layer to a higher temperature can result in undesired precipitation and agglomeration of silicon in such layer, and also adversely exposes the wafer being processed to undesired and ever increasing thermal exposure. The processing window for achieving or obtaining low resistance silicide phases for smaller line widths and contacts continues to be reduced, making fabrication difficult.

It would be desirable to develop methods which facilitate the C49 to C54 phase transformation in titanium silicide films. Although the invention was developed with an eye towards overcoming this specific problem, the artisan will appreciate applicability of the invention in other areas, with the invention only being limited by the accompanying claims appropriately interpreted in accordance with the Doctrine of Equivalents.

SUMMARY

In but one aspect, the invention provides a method of forming a crystalline phase material. In one implementation, the method is performed by providing a stress inducing material within or operatively adjacent a crystalline material of a first crystalline phase prior to anneal. The crystalline material of the first crystalline phase is annealed under conditions effective to transform it to a second crystalline phase. The stress inducing material preferably induces

compressive stress within the first crystalline phase during the anneal to the second crystalline phase to lower the required activation energy to produce a more dense second crystalline phase.

In accordance another aspect, the invention provides a method of forming a refractory metal silicide. In one implementation, the method is performed by forming a refractory metal silicide of a first crystalline phase. Compressive stress inducing atoms are provided within the refractory metal silicide of the first crystalline phase, with the compressive stress inducing atoms being larger than silicon atoms of the silicide. With the compressive stress inducing atoms within the first phase refractory metal silicide, the refractory metal silicide of the first crystalline phase is annealed under conditions effective to transform said silicide to a more dense second crystalline phase.

In another implementation, a stress inducing material is formed over the opposite side of the wafer over which the first phase crystalline material is formed.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment at one processing step in accordance with the invention.

Fig. 2 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a diagrammatic sectional view of another alternate semiconductor wafer fragment at an alternate processing step in accordance with the invention.

Fig. 4 is a view of the Fig. 3 wafer at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a diagrammatic sectional view of yet another alternate semiconductor wafer fragment at another alternate processing step in accordance with the invention.

Fig. 6 is a view of the Fig. 5 wafer at a processing step subsequent to that shown by Fig. 5.

Fig. 7 is a diagrammatic sectional view of still another alternate semiconductor wafer fragment at another alternate processing step in accordance with the invention.

Fig. 8 is a view of the Fig. 7 wafer at a processing step subsequent to that shown by Fig. 7.

Fig. 9 is a view of the Fig. 7 wafer at a processing step subsequent to that shown by Fig. 8.

Fig. 10 is a diagrammatic sectional view of another alternate semiconductor wafer fragment at another alternate processing step in accordance with the invention.

Fig. 11 is a view of the Fig. 10 wafer at a processing step subsequent to that shown by Fig. 10.

Fig. 12 is a view of the Fig. 10 wafer at a processing step subsequent to that shown by Fig. 11.

Fig. 13 is a diagrammatic sectional view of another alternate semiconductor wafer fragment at another alternate processing step in accordance with the invention.

Fig. 14 is a view of the Fig. 13 wafer at a processing step subsequent to that shown by Fig. 13.

Fig. 15 is a view of the Fig. 13 wafer at a processing step subsequent to that shown by Fig. 14.

Fig. 16 is a view of the Fig. 13 wafer at a processing step subsequent to that shown by Fig. 15.

Fig. 17 is a diagrammatic sectional view of still another alternate semiconductor wafer fragment at another alternate processing step in accordance with the invention.

Fig. 18 is a view of the Fig. 17 wafer at a processing step subsequent to that shown by Fig. 17.

Fig. 19 is a view of the Fig. 17 wafer at a processing step subsequent to that shown by Fig. 18.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring initially to Figs. 1 and 2, a semiconductor wafer fragment in process is indicated generally with reference numeral 10. Such comprises a substrate 12, for example in the form of a bulk monocrystalline silicon wafer, having an overlying crystalline material layer 14 capable of undergoing a phase transformation from a first crystalline phase to a second crystalline phase. Example materials include refractory metal silicides, such as $TiSi_x$ (where "x" ranges from 0.5 to 2.5 and is predominately "2") with a first crystalline phase being C49 and a second crystalline phase being C54. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

A layer 16 of compressive stress inducing material is provided over and in contact with (i.e., "on") first crystalline phase material 14. Layer 16 ideally has a thermal coefficient of expansion which is less

than the thermal coefficient of expansion of first crystalline phase material layer 14, particularly at a desired temperature of phase transformation. Thus, the stress induced in layer 14 at phase transformation anneal will be of a compressive nature due to the greater expansion properties of layer 14 as compared to those of layer 16. Layer 16 preferably has a thickness which is equal to or greater than a thickness of first phase crystalline material 14 to facilitate inducing desired stress. An example thickness for layers 14 and 16 is from 100 to 2000 Angstroms. Layer 16 is preferably comprised of a material that will not react with the underlying refractory metal silicide. Example and preferred materials for layer 16 include SiO_2 (doped or undoped) and Si_3N_4.

Referring to Fig. 2, first phase crystalline material layer 14 is annealed under conditions effective to transform it to a second more dense and electrically conductive crystalline phase layer 15, such as C54 TiS_x in the case of C49 titanium silicide of layer 14. The phase transformation of a refractory metal silicide from the C49 phase to the C54 phase occurs with the 7% volume reduction or density increase. Compressive stresses induced by the lesser expanding layer 16 during anneal help to facilitate phase transformation from C49 to C54 by the compressive forces facilitating this volume reduction, and reduces the required activation energy for achieving the phase transformation, which is typically in the prior art provided by temperature anneal alone. For example, one prior art processing window for achieving the desired

phase transformation is at a temperature of 800° C for a tightly controlled period of time of from 15 - 20 seconds for a 350 Angstrom thick C49 $TiSi_x$ film. Utilizing a compressive stress inducing layer 16 enables transformation to occur at temperatures less than or equal to about 750° C in an inert atmosphere (i.e., nitrogen or argon) and with less stringent time requirements, and thus potentially enables less thermal processing of the substrate being treated. An example pressure during the anneal would be from 1 Torr to 760 Torr.

The above first described preferred embodiment is but one example of a method of providing a stress inducing material (i.e., layer 16) operatively adjacent a crystalline material of a first crystalline phase (i.e. layer 14) to be effective to induce stress (i.e. in this example compressive stress) as the material is annealed to a second crystalline phase. An alternate example of providing a stress inducing material operatively adjacent a crystalline material to be transformed to a secondary crystalline phase is to provide such stress inducing material under or inwardly of the first crystalline phase material, as described with reference to Figs. 3 - 4. Such illustrates a semiconductor wafer fragment in process generally with reference numeral 18. In Fig. 3, such comprises a substrate 20, for example bulk monocrystalline silicon or layers of material, having an overlying stress inducing material layer 22. A layer 24 of crystalline material of the first crystalline phase is provided outwardly of layer 22, with layer 22 thus being inwardly of or under layer 24 and in the illustrated example in contact

Sub E' (Cont'd)

therewith. In the example refractory metal silicide transformation of a C49 phase to a C54 phase accompanied by a volume reduction, layer 22 ideally also has a coefficient of expansion which is less than the coefficient of expansion of layer 24. Such facilitates putting layer 24 in compressive stress during phase transformation. Example materials include those provided above for layer 16.

Referring to Fig. 4, annealing is conducted as in the first described embodiment to transform first crystalline phase material layer 24 into a more dense and higher electrically conductive second phase material layer 25.

Yet another alternate example is described with reference to Figs. 5 and 6. Here, the stress inducing material is provided within the crystalline material undergoing phase transformation. Fig. 5 illustrates a wafer fragment 30 comprised of some substrate construction 32. Again, such could be a monocrystalline silicon substrate or some other substrate assembly atop monocrystalline silicon or some other material. A crystalline material of a first crystalline phase 34, such as a refractory metal silicide, is formed outwardly of substrate 32. An example technique, as with the above described embodiment, is by chemical vapor deposition. Alternate examples of providing first phase crystalline materials for layers 14, 24 and 34 of the first described embodiments will be described below. Compressive stress inducing atoms 36 are provided within first crystalline phase material layer 34. Where layer 34 comprises a refractory metal silicide, atoms 36

advantageously are provided to be larger than silicon atoms of the silicide to produce desired compressive stress during the anneal to produce the volume reduced phase transformation. Such example atoms include Ge, W and Co or mixtures thereof. One example technique for providing atoms 36 within layer 34 is by ion implantation or gas diffusion. An example concentration range is from 10^{16} - 10^{22} atoms/cm^3.

Referring to Fig. 6, the refractory metal silicide of the first crystalline phase is annealed under conditions effective to transform silicide to a more dense second crystalline phase layer 35, with atoms 36 inducing compressive stress during such anneal. Anneal conditions as described above are preferred.

Thus, the above described embodiments provide alternate examples of providing stress inducing material proximate (either within or operatively adjacent) a crystalline material of a first crystalline phase which is to undergo phase transformation to a second crystalline phase. In the described and preferred embodiment, such is accompanied by a volume reduction such that the stress induced is desirably of a compressive nature. The above two techniques could of course also be combined such that the stress inducing material is provided both within and operatively adjacent the material undergoing phase transformation. Further, the stress inducing material layer might be provided prior to the subject layer being transformed being at the first crystalline phase conditions. For example, refractory metals when deposited over silicon

containing layers, such as polysilicon, undergo chemical transformation to silicides merely under elevated temperature anneal conditions. In each of the above described embodiments, the stress inducing material was provided after the silicide material of the first crystalline phase came into existence. An alternate example whereby the stress inducing material is provided before the first phase crystalline material comes into existence is initially described with reference to Fig. 7 - 9.

Fig. 7 illustrates a wafer fragment 38 comprised of a substrate in the illustrated form of a silicon, SiO_2 or other material substrate 40 having an overlying stress inducing material layer 42, such as SiO_2 or Si_3N_4. An example thickness for layer 42 is from 100 - 2000 Angstroms. A polysilicon layer 44 of an example thickness of from 100 - 2000 Angstroms is provided outwardly of stress inducing material layer 44. Outwardly thereof is provided a refractory metal layer 46, such as elemental titanium. Thus, a refractory metal (i.e., layer 46) is formed on a silicon containing substrate (i.e. layer 44). The thickness of layer 42 is preferably greater than or equal to the combined thickness of layers 44 and 46.

Referring to Fig. 8, wafer 38 is annealed to impart a reaction to form a refractory metal silicide layer 48 of, for example, the first C49 crystalline phase from the refractory metal of layer 46 and the silicon of the underlying substrate 44. Example anneal conditions include 600°C, 760 Torr in an inert N_2 or Ar ambient for 20 seconds.

Referring to Fig. 9, refractory metal silicide layer 48 of the first crystalline phase is annealed to transform the first phase silicide to a more dense second crystalline phase layer 49. Example anneal conditions for such phase transformation are as described above with respect to the first described embodiments. Alternately, the wafer fragment of Fig. 7 could inherently be subjected to the second phase transformation anneal conditions at the outset, wherein the wafer being processed would inherently be transformed initially to the Fig. 8 embodiment and subsequently to the Fig. 9 embodiment.

The above described embodiment with respect to Figs. 7 - 9 could of course also be utilized in conjunction with the Figs. 5 and 6 embodiment wherein the stress inducing material is provided within the first crystalline phase material. For example, the compressive stress inducing atoms can be provided *in situ* into a refractory metal layer during its deposition over an underlying silicon containing substrate. Such could be provided for example by sputtering or chemical vapor deposition such that the atoms are received within the deposited refractory metal layer. Alternately, ion implanting or gas diffusion doping could be utilized. An example concentration range for the stress inducing atoms is as described above, namely from 10^{16} - 10^{22} atoms/cm^3. Subsequently, the refractory metal layer having the atoms therein would be annealed to form the refractory metal silicide of the first crystalline phase from the reaction of the refractory metal and underlying silicon. Continued or subsequent annealing with the stress

inducing atoms in place will facilitate phase transformation to the second phase.

Another alternate embodiment is described with reference to Figs. 10-12 whereby the stress inducing layer is provided over or outwardly of, and thereby operatively adjacent, the titanium layer prior to its initial transformation to the first C49 crystalline phase. Fig. 10 illustrates a semiconductor wafer fragment 50 comprised of a bulk monocrystalline silicon substrate and an overlying insulating layer 54, such as SiO_2. A polysilicon layer 56 is provided outwardly of layer 54, with a refractory metal layer 58, such as titanium, provided outwardly of polysilicon layer 56. A compressive stress inducing layer 60 is provided over and on titanium layer 58 and preferably has a thickness equal to or greater than the combined thickness of layers 56 and 58.

Referring to Fig. 11, suitable annealing conditions for example as described above are utilized to transform layers 56 and 58 into a C49 first crystalline phase layer 61.

Referring to Fig. 12, subsequent or continued suitable annealing transforms first crystalline phase material layer 61 into second C54 crystalline phase material layer 63, with the presence of compressive stress inducing layer 60 facilitating such phase transformation as described above.

The above described embodiments can be utilized in contact or any other technologies where refractory metal silicides or other crystalline materials are formed. An example embodiment in utilizing

aspects of the above process in fabricating of electrically conductive lines is described with reference to Figs. 13 - 16.

Referring to Fig. 13, a wafer fragment 65 comprises a bulk monocrystalline silicon substrate 66 having a gate oxide layer 68 provided thereover. A layer of polysilicon 70 is provided outwardly of gate oxide layer 68 with a silicide layer 72 of a C49 first crystalline phase provided outwardly of polysilicon layer 70. Such can be provided by the above or other conventional techniques. Thus, a semiconductive material (i.e. silicon of layer 70) is provided over a substrate, (i.e. material 68 and 66), with a refractory metal silicide 72 of a first crystalline phase being provided over and in ohmic electrical connection with the semiconductive materials. Layer 70 is desirably conductively doped with a suitable conductively enhancing impurity either at this point or subsequent in the processing.

Referring to Fig. 14, layers 72, 70 and 68 are patterned into conductive lines 74 and 76.

Referring to Fig. 15, a compressive stress inducing material layer 78 is formed outwardly of lines 74 and 76, preferably to a thickness at least as great as silicide portion 72. Again, preferred materials include SiO_2 or Si_3N_4.

Referring to Fig. 16, the wafer fragment is annealed as above to transform the silicide material 72 of the first crystalline phase to C54 second crystalline phase material 80. Layer 78 can remain, be removed,

anisotropically etched or otherwise processed as the circuitry design dictates.

The above described Figs. 13-16 embodiment is a technique whereby the conductive line patterning (in this example a gate line) is conducted before the annealing, and the compressive stress inducing material is provided after the line patterning. Alternately, the patterning can be conducted after the annealing. Further, compressive stress inducing material can be provided within the first crystalline phase refractory metal silicide layer 72 as is for example described with reference to the Figs. 5 and 6 embodiment. Alternate techniques are also of course contemplated, as will be appreciated by the artisan.

A further alternate embodiment is described with reference to Figs. 17 - 19. Fig. 17 illustrates a semiconductor wafer fragment 83 (such as monocrystalline silicon) having opposing first and second sides 84 and 85, respectively.

Referring to Fig. 18, a crystalline material layer 87 of a first crystalline phase (such as the exemplary C49 $TiSi_X$) is formed over first wafer side 84. A compressive stress inducing material layer 89 is provided over and on second wafer side 85. Layer 89 is provided to have a thermal coefficient of expansion which exceeds that of layer 87. An example material where layer 87 comprises a refractory metal silicide is TiN.

Referring to Fig. 19, wafer 83 is annealed under conditions such as that described above to transform first phase material 87 into second

phase material 91. The greater coefficient of layer 89 as compared to layer 87 causes a degree of bowing which effectively places layer 87 in compressive stress to facilitate its transformation to layer 91.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.